

#2

Form 1449*	Atty. Docket No.: 303.506US4	Serial No. <del>Unknown</del> 10/057225
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes	
	Filing Date: Herewith	Group: <del>Unknown</del> 2822

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
MT	4,287,083	09/01/1981	McDowell, J.R., et al.	252	182	06/18/79
MT	4,605,909	08/12/1986	Tsironis, C.	331	96	01/28/82
MT	5,006,909	04/09/1991	Kosa, Y.	357	23.6	10/30/89
MT	5,057,896	10/01/1991	Gotou, H.	357	49	05/30/89
MT	5,391,895	02/21/1995	Dreifus, D.L.	257	77	09/21/92
MT	5,585,288	12/17/1996	Davis, S.E., et al.	438	38174	07/16/90
MT	5,661,424	08/26/1997	Tang, D.D.	327	105	01/27/93

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
MT	4370978	12/24/1992	Japan	H01L	29/784	X
MT	60-116163	06/22/1985	Japan	H01L	27/08	X

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial	
MT	GaAs IC Symposium, IEEE Gallium Arsenide Integrated Circuit Symposium, 19th Annual Technical Digest, Anaheim, California, pgs. 1 - 290, (October 12-15, 1997)
MT	Asai, S., et al., "The GaAs Dual-Gate Fet With Low Noise And Wide Dynamic Range", Technical Digest, International Electron Devices Meeting, pgs. 64-67, (December 1973)
MT	Colinge, J.P., "Reduction of Kink Effect in Thin-Film SOI MOSFET's", IEEE Electron Device Letters, 9(2), pgs. 97 - 99, (1988)
MT	Denton, J.P., et al., "Fully Depleted Dual-Gated Thin-Film SOI P-MOSFET's Fabricated in SOI Islands with an Isolated Buried Polysilicon Backgate", IEEE Electron Device Letters, 17(11), pp. 509-511, (November 1996)
MT	Mizuno, T., et al., "High Speed and Highly Reliable Trench MOSFET with Dual-Gate", 1988 Symposium on VLSI Technology, Digest of Technical Papers, pp. 23-24, 991, (1988)
MT	Nishinohara, K., et al., "Effects of Microscopic Fluctuations in Dopant Distributions on MOSFET Threshold Voltage", IEEE Transactions on Electron Devices, 39(3), pgs. 634-639, (March 1992)

Examiner Michael Trinh	Date Considered 8/22/02
------------------------	-------------------------

\*Substitute Disclosure Statement Form (PTO-1449)

\*\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.506US4	Serial No. <del>Unknown</del>
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes	10/057,225
	Filing Date: Herewith	Group: <del>Unknown</del> 2822

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

\*\*Examiner  
Initial

1050 U.S. PTO  
10/057225  
01/25/02

MT	Stolk, P.A., et al., "The Effect of Statistical Dopant Fluctuations on MOS Device Performance", <u>IEEE</u> , pgs. 23.4.1 - 23.4.4, (1996)
	Sze, S.M., <u>In: Physics of Semiconductor Devices, Second Edition</u> , Wiley-Interscience Publications, John Wiley & Sons, New York, p. 362-279, 433-438, (1981)
	Takeuchi, K., et al., "Channel Engineering for the Reduction of Random-Dopant-Placement-Induced Threshold Voltage Fluctuations", <u>IEEE</u> , pgs. 33.6.1 - 33.6.4, (1997)
	Taur, Y., et al., "CMOS Devices below 0.1 micrometer: How High Will Performance Go?"  ", <u>IEEE</u> , pgs. 9.1.1 - 9.1.4, (1997)
	Wong, H.S., et al., "Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel", <u>IEEE</u> , pgs. 16.6.1 - 16.6.4, (1997)
MT	Wong, H.S., et al., "Three-Dimensional "Atomistic" Simulation of Discrete Random Dopant Distribution Effects in Sub-0.1 micrometer MOSFET's", <u>IEEE</u> , pgs. 29.2.1- 29.2.4, (1993)

Examiner <u>Michael Trink</u>	Date Considered <u>8/22/02</u>
-------------------------------	--------------------------------

\*Substitute Disclosure Statement Form (PTO-1449)

\*\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.